WE CLAIM:

1. A method of fabricating trench isolation structures between integrated electrical devices in a semiconductor substrate, comprising:

placing a semiconductor substrate in a reaction chamber, the semiconductor substrate comprising trenches; and

filling the trenches with insulating material by atomic layer deposition, comprising a plurality of primary cycles, each primary cycle comprising, in sequence:

introducing a first vapor-phase reactant to the substrate, thereby forming no more than about one monolayer of a first reactant species conforming at least to surfaces of the trenches;

removing excess first vapor-phase reactant and byproduct from the reaction chamber;

introducing a second vapor-phase reactant to the substrate, thereby reacting with the first reactant species conforming at least to the surfaces of the trenches; and

removing excess second vapor-phase reactant and byproduct from the reaction chamber.

2. The method of Claim 1, wherein the first vapor-phase reactant comprises a silicon source gas and the second vapor-phase reactant comprises an oxidant source gas.

3. The method of Claim 2, wherein filling the trenches comprises repeating the primary cycles until the trenches are filled.

4. The method of Claim 2 wherein the primary cycles are repeated until no space remains within the trenches.

5. The method of Claim 4, wherein the silicon source gas comprises a species of aminoalkyltrialkoxysilane and the oxidant source gas comprises ozone.

6. The method of Claim 1, wherein filling the trenches further comprises a plurality of secondary cycles, each secondary cycle comprising, in sequence:

introducing a third vapor-phase reactant to the substrate, thereby forming no more than about one monolayer of a third reactant species conforming at

least to surfaces of the trenches, the third reactant species being different from the first reactant species;

removing excess third vapor-phase reactant and byproduct from the reaction chamber;

introducing a fourth vapor-phase reactant to the substrate, thereby reacting with the third reactant species conforming at least to the surfaces of the trenches; and

removing excess fourth vapor-phase reactant and byproduct from the reaction chamber.

7. The method of Claim 6, wherein the first vapor-phase reactant comprises a silicon source gas, the third vapor-phase reactant comprises an aluminum source gas and the second and fourth vapor-phase reactants comprise oxidant source gases.

8. The method of Claim 7, wherein the aluminum source gas comprises alkyl aluminum compounds and the oxidant source gas comprises water.

9. The method of Claim 7, wherein filling the trench consists of mixing the primary cycle and secondary cycle in a primary cycle to secondary cycle ratio between about 20:1 and 1:10.

10. The method of Claim 6, wherein the primary cycles deposit a first oxide species and the secondary cycles deposit a second oxide species.

11. The method of Claim 10, wherein the first oxide species is silicon oxide and the second oxide species is a metal oxide.

12. The method of Claim 11, wherein the second oxide species is aluminum oxide.

13. The method of Claim 12, wherein filling the trench comprises depositing between about 23% and 37% aluminum oxide by weight in silicon oxide.

14. The method of Claim 12, wherein filling the trench comprises depositing between about 26% and 34% aluminum oxide by weight in silicon oxide

15. The method of Claim 10, wherein at least a portion of the first and second oxide species combine to form a separate phase in equilibrium with a portion of the first oxide.

16. The method of Claim 15, wherein the separate phase comprises mullite, the first oxide comprises silicon oxide and the second oxide comprises aluminum oxide.

17. The method of Claim 16, wherein the insulating material comprises between about 25% mullite and 50% mullite by weight.

18. The method of Claim 10, wherein the primary and secondary cycles are mixed in a ratio to match a coefficient of thermal expansion (CTE) of the insulating material to within about 20% of a CTE of the semiconductor substrate.

19. The method of Claim 18, wherein the primary and secondary cycles are mixed in a ratio to match a coefficient of thermal expansion (CTE) of the insulating material to within about 10% of a CTE of the semiconductor substrate.

20. A method for forming a trench isolation structure in an integrated circuit, comprising:

forming a trench in a semiconductor substrate; and

filling the trench with an insulating material comprising a mixture of silicon oxide and aluminum oxide.

21. The method of Claim 20, wherein the insulating material contains between about 23% and 37% by weight aluminum oxide in silicon oxide.

22. The method of Claim 20, wherein filling the trench comprises depositing silicon oxide and aluminum oxide by atomic layer deposition.

23. The method of Claim 22, wherein filling the trench comprises mixing atomic layer deposition cycles in a ratio of silicon oxide cycles to aluminum oxide cycles between about 20:1 and 1:10.

24. The method of Claim 20, further comprising removing the insulating material from a top surface of the silicon substrate and leaving the insulating material within the trench.

25. The method of Claim 20, wherein filling the trench comprises depositing silicon oxide and aluminum oxide in a ratio to form a material with a coefficient of thermal expansion within about 20% of a coefficient of thermal expansion for the silicon substrate.

26. The method of Claim 25, wherein filling the trench comprises depositing silicon oxide and aluminum oxide in a ratio to form a material with a coefficient of

thermal expansion within about 10% of the coefficient of thermal expansion for the silicon substrate.

27. The method of Claim 20, wherein the insulating material comprises a mixture of mullite and silicon oxide phases.

28. A method of fabricating a trench-fill structure in an integrated circuit, comprising:

forming a trench within a structural material in a partially fabricated integrated circuit;

depositing a first filler material by a plurality of primary atomic layer deposition cycles, each cycle depositing no more than about one monolayer of the first filler material;

depositing a second filler material by a plurality of secondary atomic layer deposition cycles, each cycle depositing no more than about one monolayer of the second filler material; and

performing the primary and secondary cycles a number of times to fill the trench, a ratio of primary cycles to secondary cycles selected to form a composite filler material having a coefficient of thermal expansion within about 20% of a coefficient of thermal expansion of the structural material.

29. The method of Claim 28, wherein at least a portion of the first filler material and the second filler material form a third phase in equilibrium with a portion of the first filler material.

30. The method of Claim 28, wherein the ratio is selected so that the composite filler material has a coefficient of thermal expansion with about 10% of the coefficient of thermal expansion of the structural material.

31. The method of Claim 28, wherein the structural material comprises a silicon substrate and the composite filler material serves as a device isolation element between transistor active areas within the silicon substrate.

32. The method of Claim 31 wherein the first filler material comprises silicon oxide.

33. The method of Claim 31 wherein the second filler material comprises aluminum oxide.

34. A process for filling a trench with an insulator for isolating active areas within a semiconductor substrate, comprising:

providing the semiconductor substrate, with a trench formed therein, in a reaction chamber;

providing a carrier gas flow through the reaction chamber;

alternatingly injecting an aluminum source gas pulse and an oxidant source gas pulse into the carrier gas flow in a plurality of alumina cycles, each alumina cycle depositing no more than about one monolayer of aluminum oxide in a self-saturating reaction;

alternatingly injecting a silicon source gas pulse and an oxidant source gas pulse into the carrier gas flow in a plurality of silica cycles, each silica cycle depositing no more than about one monolayer of silicon oxide in a self-saturating reaction; and

mixing the alumina and silica cycles to fill the trench with a two-phase material.

35. The process of Claim 34, wherein the alumina cycles and silica cycles are applied in a ratio to produce the insulator with a coefficient of thermal expansion within about 20% of a coefficient of thermal expansion of the semiconductor substrate.

36. The process of Claim 34, wherein the aluminum source gas is selected from the group consisting of aluminum halides, alkyl aluminum compounds, trimethyl aluminum, aluminum alkoxides, aluminum ethoxide, aluminum beta-diketonates and anhydrous aluminum nitrate.

37. The process of Claim 36, wherein the silicon source gas is selected from the group consisting of silicon halides, halosilanes and organic silicon compounds.

38. The process of Claim 34, wherein mixing the alumina and silica cycles comprises using a ratio of silica cycles to alumina cycles of between about 20:1 and 1:10.

39. The process of Claim 38, wherein mixing the alumina and silica cycles comprises using a ratio of silica cycles to alumina cycles of between about 10:1 and 3:1.

40. The process of Claim 34, wherein the a two-phase material comprises a mixture of silicon oxide and mullite.

41. The process of Claim 34, wherein a temperature of the semiconductor substrate is between about 200°C and 400°C.

42. The process of Claim 41, wherein the temperature of the semiconductor substrate is kept constant during the alumina and silica cycles.

43. An integrated circuit, comprising:

a semiconductor substrate with a plurality of neighboring active device regions;

openings embedded within the semiconductor substrate between the neighboring active device regions; and

an insulating material that fills the openings conformally, the insulating material comprising a mixture of silica and mullite.

44. The integrated circuit of Claim 43, wherein a ratio of mullite to silica in the insulating material is between about 25 wt % mullite/75 wt % silica to about 50 wt % mullite/50 wt % silica.

45. The integrated circuit of Claim 46, wherein a ratio of mullite to silica in the insulating material is between about 35 wt % mullite/65 wt % silica to about 40 wt % mullite/60 wt % silica.

46. The integrated circuit of Claim 43, wherein the insulating material has a coefficient of thermal expansion between about 2.0×10^{-6} /K and 3.0×10^{-6} /K.

47. The integrated circuit of Claim 46, wherein the insulating material has a coefficient of thermal expansion between about 2.25×10^{-6} /K and 2.75×10^{-6} /K.

48. The integrated circuit of Claim 43, wherein the openings have an aspect ratio greater than about 3:1.

49. The integrated circuit of Claim 48, wherein the openings have an aspect ratio greater than about 5:1.

50. The integrated circuit of Claim 43, wherein the openings are narrower than about 100 nm.

51. A trench isolation structure in an integrated circuit, comprising:

an opening embedded within a semiconductor substrate between neighboring devices; and

an insulating material that fills the opening conformally and that has a linear coefficient of thermal expansion within about 20% of a linear coefficient of thermal expansion of the semiconductor substrate.

52. The trench isolation structure of Claim 51, wherein the semiconductor substrate is silicon and the insulating material comprises a mixture of silica and mullite.

53. The trench isolation structure of Claim 52, wherein the insulating material contains between about 25 weight percent and 50 weight percent mullite.

54. The integrated circuit of Claim 53, wherein the insulating material contains between about 35 weight percent and 40 weight percent mullite.

55. The trench isolation structure of Claim 51, wherein the insulating material is a mixture of silica and alumina having between about 23% and 37% aluminum oxide.

56. The trench isolation structure of Claim 55, wherein the insulating material has between about 26% and 34% alumina by weight.

57. The trench isolation structure of Claim 51, wherein the insulating material comprises a mixture of at least two oxide phases selected to have a coefficient of thermal expansion that matches the semiconductor substrate.

58. The trench isolation structure of Claim 51, wherein the insulating material that fills the opening conformally contains no voids.